J1998 U.S. PTO 10/050417 01/16/02

PATENT NUMBER and ISSUE DATE

# U.S. UTILITY Patent Application

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| APPL NUM | FILING DATE | CLASS | SUBCLASS | GAU | EXAMINER |
|---|---|---|---|---|---|
| 10050417 | 01/16/2002 | ~~438~~ | 311 | ~~2812~~ | ~~[illegible]~~ |

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**CONTINUING DATA VERIFIED:

THIS APPLN CLAIMS BENEFIT OF 60/285,197 04/20/2001

** FOREIGN APPLICATIONS VERIFIED:

| PG-PUB | DO NOT PUBLISH ☐ | RESCIND ☐ | |
|---|---|---|---|
| Foreign priority claimed | ☐ yes ☐ no | ATTORNEY DOCKET NO | |
| 35 USC 119 conditions met | ☐ yes ☐ no | G0131 | |
| Verified and Acknowledged Examiner's Initials | | | |

TITLE : Methods and systems for controlling resist residue defects at gate layer in a semiconductor device manufacturing process

| NOTICE OF ALLOWANCE MAILED | | Assistant Examiner | CLAIMS ALLOWED | |
|---|---|---|---|---|
| | | | Total Claims | Print Claim for O.G. |
| ISSUE FEE | | | DRAWING | | |
| Amount Due | Date Paid | | Sheets Drwg. | Figs. Drwg. | Print Fig. |
| | | Primary Examiner | | | |
| ☐ TERMINAL DISCLAMER | | PREPARED FOR ISSUE | Application Examiner | | |

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